

FPGA & digital design

Digital design from architecture and RTL through simulation and hardware integration. We build custom peripherals, data paths, and processor-connected logic around explicit timing and interface requirements.

WHAT WE CAN DO

- 01

RTL architecture

Control logic, pipelines, state machines, and resource allocation translated from a clear functional specification.
- 02

Processor integration

Register maps, interrupt behavior, and bus interfaces that connect custom logic to embedded software.
- 03

Data & display pipelines

Serial interfaces, CRC logic, pixel pipelines, and buffering designed around data-flow requirements.
- 04

Verification & timing

Testbenches, simulation, formal checks where appropriate, and implementation review against target constraints.

TECHNOLOGIES & WORKING AREAS

Verilog / VHDL / RISC-V softcores / AXI4-Lite / SPI / GHDL / simulation / Formal verification

A CLEAR PATH TO HANDOVER.

WHAT YOU RECEIVE

- RTL source and interface specification
- Simulation testbenches and test evidence
- Synthesis and implementation configuration
- Register-level integration documentation
- Hardware demonstration and handover notes

HOW THE WORK PROGRESSES

- 01 Specify behavior**
Clocks, interfaces, data rates, and acceptance cases.
- 02 Design the logic**
Partition the data path and control architecture.
- 03 Simulate & implement**
Check behavior, resource use, and timing.
- 04 Integrate & verify**
Connect firmware and validate on the target.

RELEVANT ENGINEERING

RV32IMC FreeRTOS SoC

PicoRV32 adaptation, compressed instructions, and a custom FreeRTOS port.

FPGA HDMI Tile Engine

A tile-based 640 x 480 HDMI pipeline controlled over SPI by STM32.

TO SCOPE YOUR PROJECT

- / FPGA family and development board
- / Clock and interface requirements
- / Expected data rates and resource budget
- / Host software or integration constraints

LET'S DISCUSS YOUR PROJECT

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